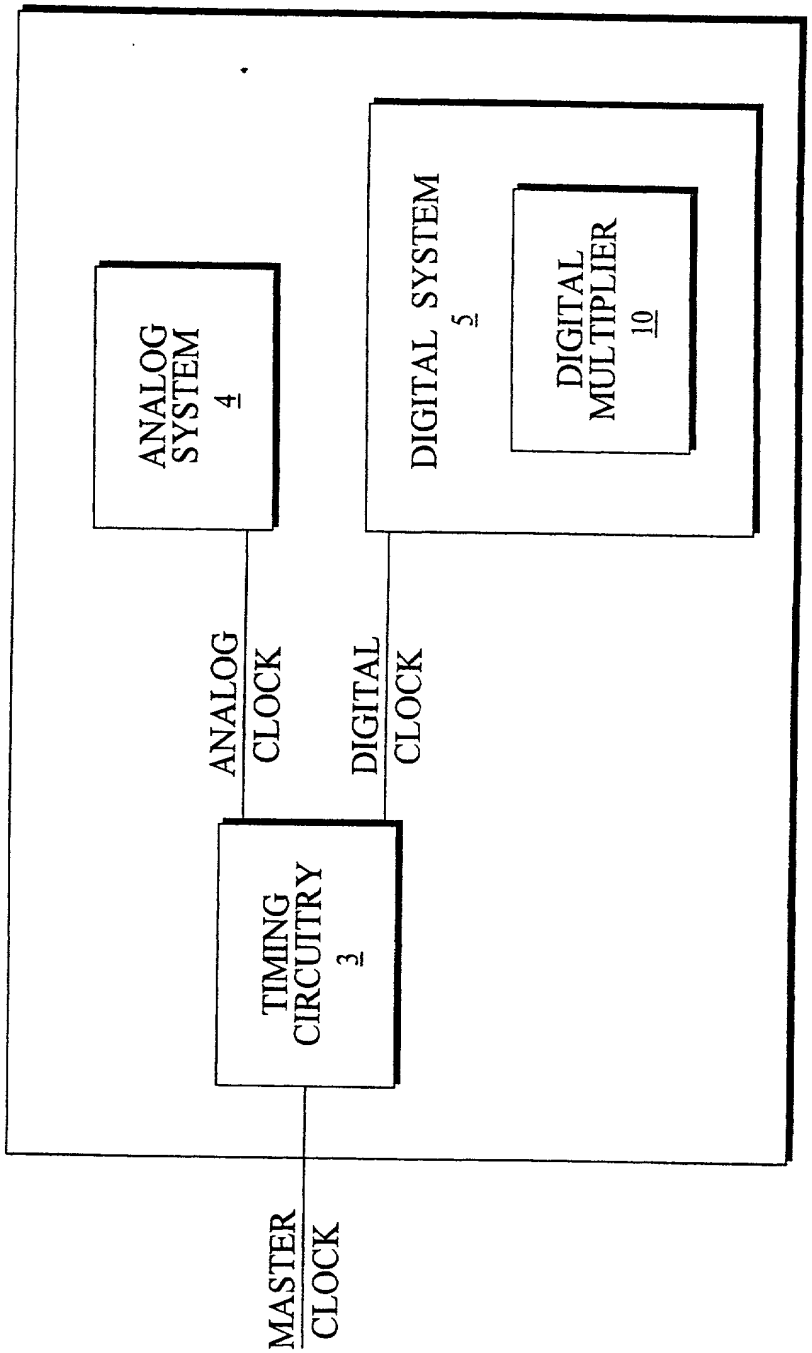

ANALOG SYSTEM 4
DIGITAL SYSTEM 5
DIGITAL MULTIPLIER 10
ANALOG CLOCK
DIGITAL CLOCK
TIMING CIRCUITRY 3
MASTER CLOCK

Fig. 1

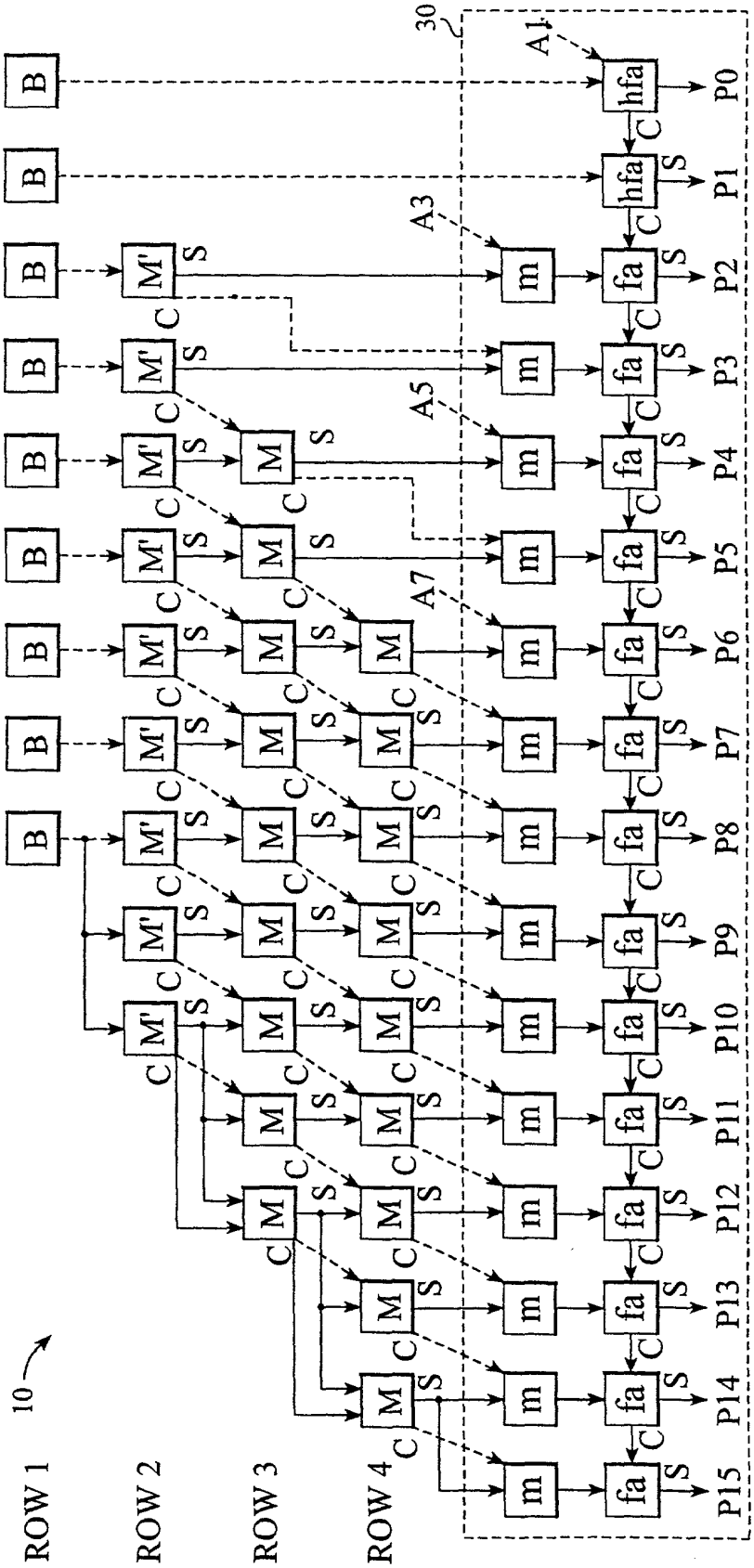
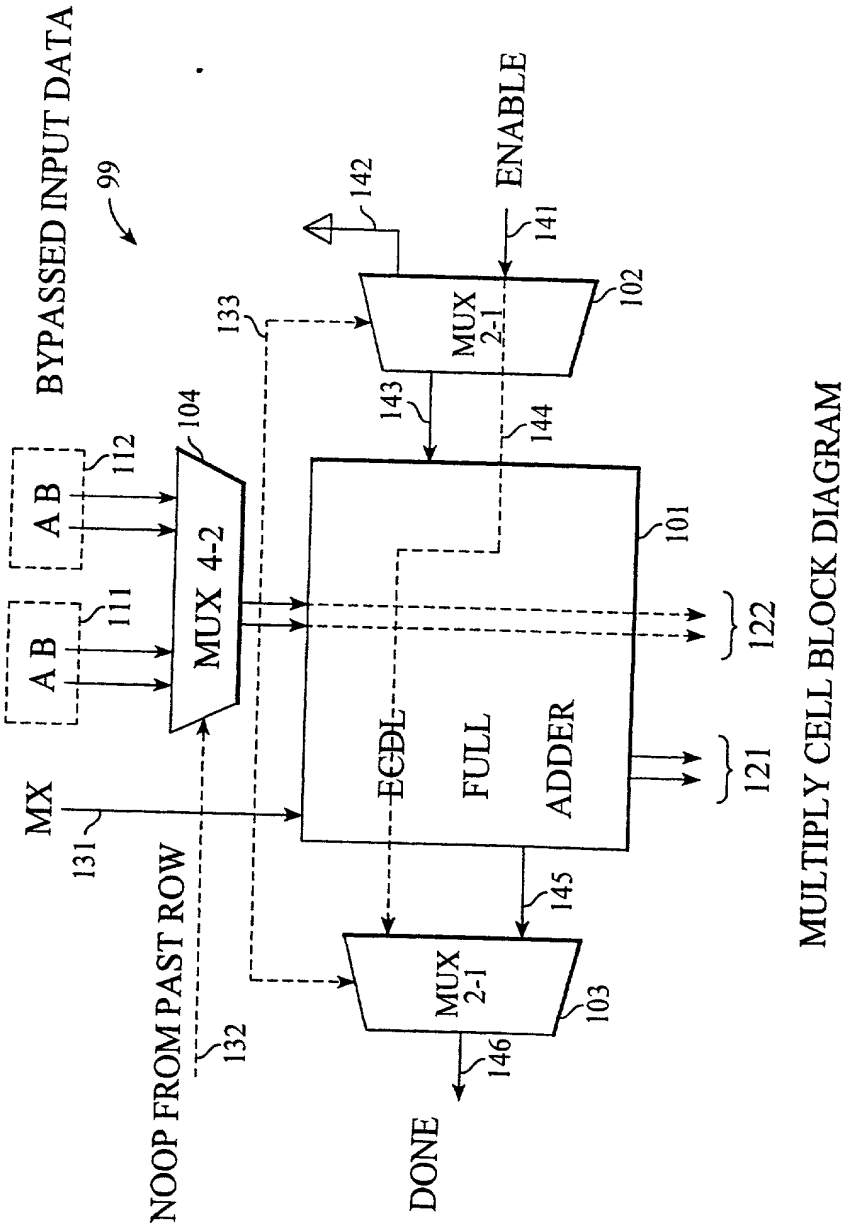

ROW 1
ROW 2
ROW 3
ROW 4
10
30
A1
A3
A5
A7
B
M'
M
m
fa
hfa
C
S
P0
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15

Fig. 2



MULTIPLY CELL BLOCK DIAGRAM

Fig. 3

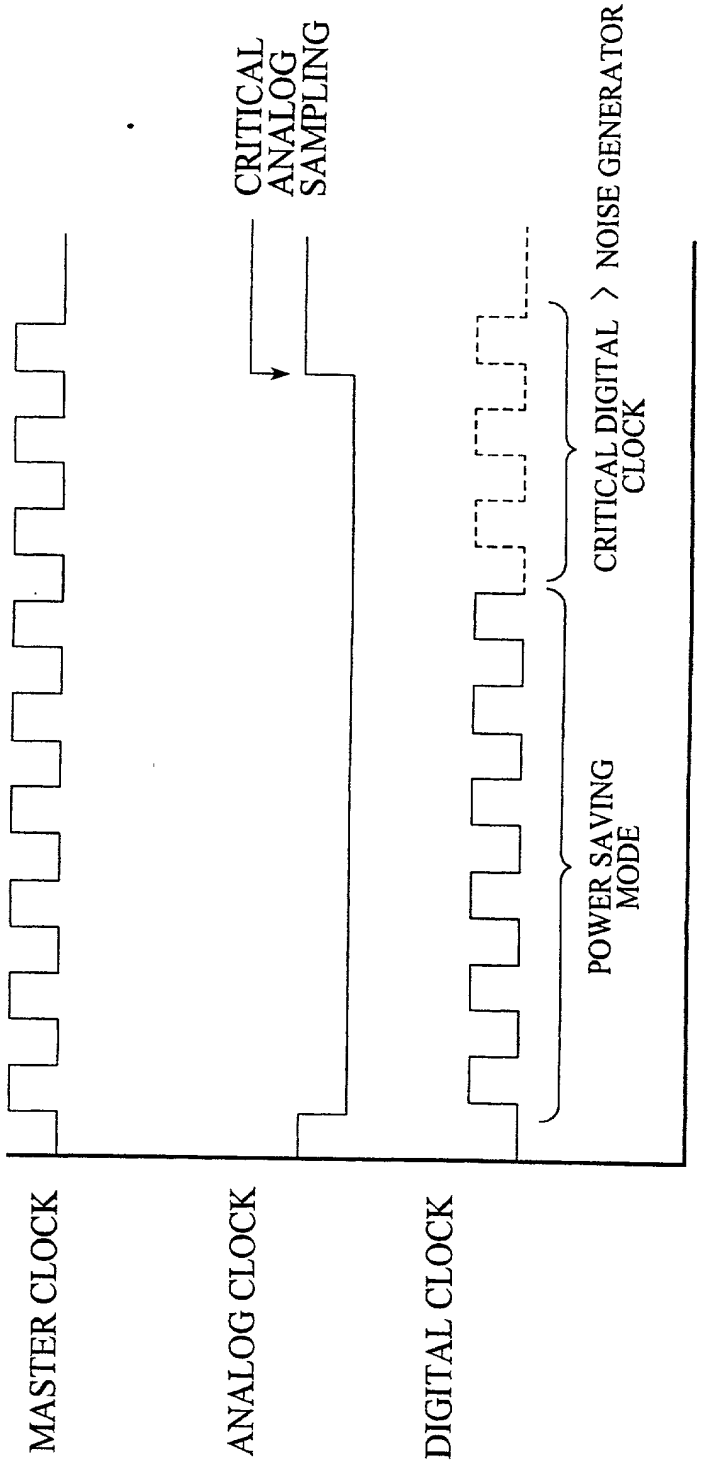

MASTER CLOCK
ANALOG CLOCK
DIGITAL CLOCK
CRITICAL ANALOG SAMPLING
POWER SAVING MODE
CRITICAL DIGITAL CLOCK
NOISE GENERATOR

Fig. 4

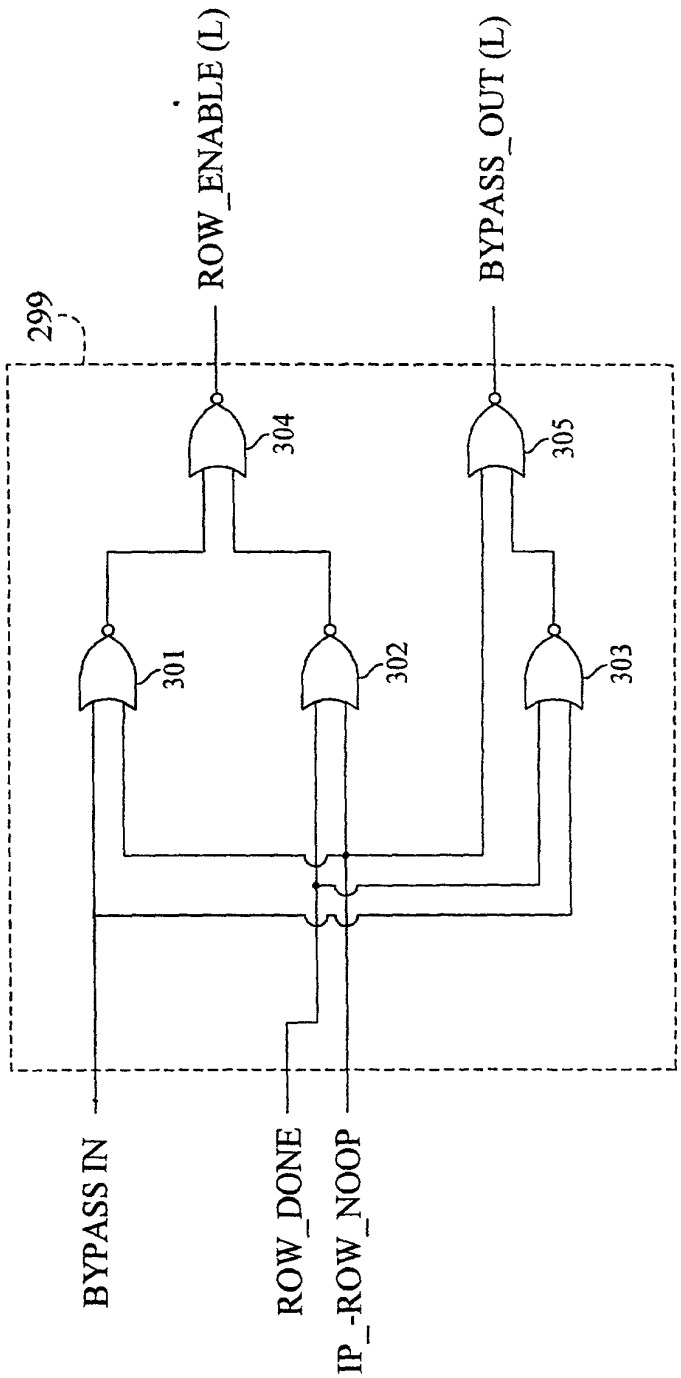


Fig. 5 (Prior Art)

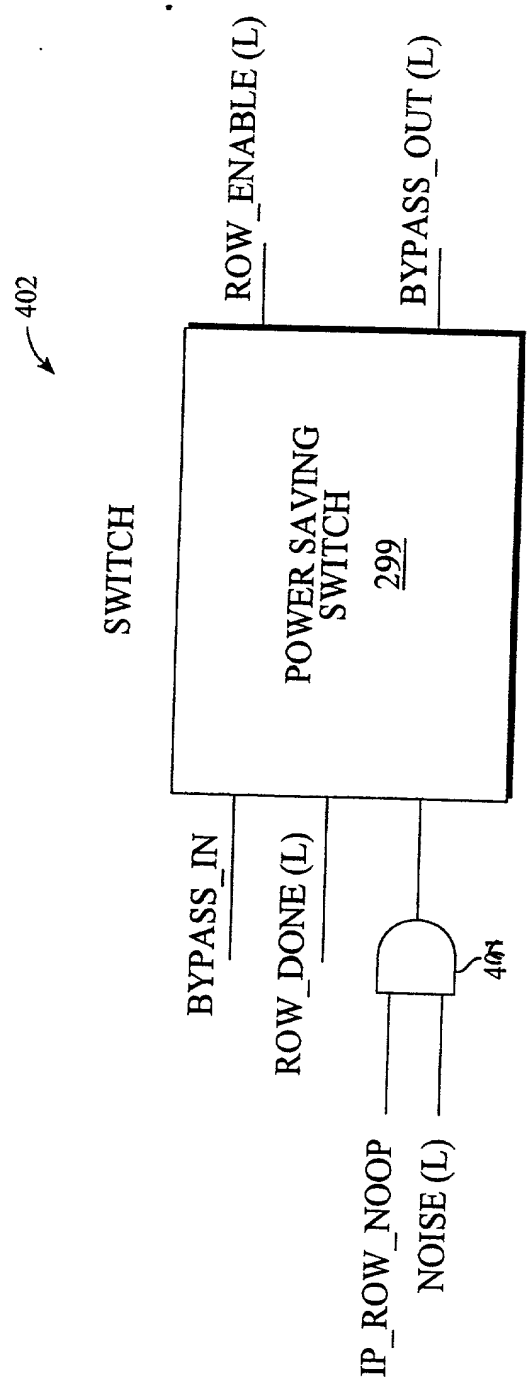

402
SWITCH
POWER SAVING SWITCH
299
ROW_ENABLE (L)
BYPASS_OUT (L)
BYPASS_IN
ROW_DONE (L)
IP_ROW_NOOP
NOISE (L)

Fig. 6